SUPPORT FOR AMENDMENTS

Support for the amendments herein can be found throughout the specification, Title and Abstract as originally filed. Additional support for the amendment to page 10, lines 3-14 (more particularly lines 5-6) can be found at http://tess.uspto.gov/. (See attached printout of the "PSOC" trademark registration information therein.) No new matter is introduced.

REMARKS

Claims 1-23 are presented for consideration in the present application, which is now believed to be in condition for examination. Early notice to that effect is earnestly solicited.

Respectfully submitted,

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AMENDMENTS WITH CHANGES SHOWN:

IN THE TITLE

[PSoC] PROGRAMMABLE MICROCONTROLLER ARCHITECTURE (MIXED ANALOG/DIGITAL)

IN THE SPECIFICATION

At page 2, line 2:

[PSoC] PROGRAMMABLE MICROCONTROLLER ARCHITECTURE (MIXED ANALOG/DIGITAL)

At page 4, line 2 through page 5, line 11:

Accordingly, the present invention provides a microcontroller consisting of programmable analog blocks and programmable digital blocks interconnected with a programmable interconnect structure fabricated on a single semiconductor chip. [Programmable System On-a-Chip (PSoC)] A programmable mixed analog/digital architecture offers an excellent analog and digital interface that solves many design needs. The present design provides the complex communication interface between digital and analog blocks that can be reconfigured on-the-fly. The programmable analog array with both Continuous Time (CT) analog blocks and Switched Capacitor (SC) analog blocks are realized on the same semiconductor chip with programmable digital blocks.

A microcontroller with a mixed programmable analog/digital [Programmable System On-a-Chip (PsoC)] architecture including multiple digital [PSoC] programmable blocks and multiple analog [PSoC] programmable blocks in a communication array having a programmable interconnect structure is described. The single chip design is implemented by integration of programmable digital and analog circuit blocks that are able to communicate with each other. Robust analog and digital blocks that are flash memory programmable can be utilized to realize complex design applications that otherwise would require multiple chips and/or separate applications. The [PSoC] programmable microcontroller architecture includes a novel array having programmable digital blocks that can communicate with programmable analog blocks using a programmable interconnect structure. The programmable analog array contains a complement of Continuous Time (CT) blocks and a complement of Switched Capacitor (SC) blocks that can communicate together. The analog blocks consist of multi-blocks that can communicate together. The analog blocks consist of multi-function circuits programmable for one or more different analog functions, and fixed function circuits programmable for a fixed function with variable parameters. The digital blocks include standard multi-function circuits and enhanced circuits having functions not included in the standard digital circuits. The [PSoC] programmable array is programmed by flash memory and programming allows dynamic reconfiguration. That is, "on-the-fly" reconfiguration of the [PsoC] programmable blocks is allowed. The programmable analog array with both Continuous Time analog blocks and Switched Capacitor analog blocks are offered on a single chip along with programmable digital

blocks. The programmable interconnect structure provides for communication of input/output data between all analog and digital blocks.

At page 7, lines 3-15:

Figure 1 is a block diagram illustrating the architecture of [the Programmable System On-a-Chip (PsoC)] a programmable array according to the present invention.

Figure 2 illustrates one embodiment of the hardware routing resources of [the Programmable System On-a-Chip (PsoC)] a programmable architecture according to the present invention.

Figure 3 is a flow chart illustrating steps in a combined digital/analog operation possible with [the Programmable System On-a-Chip (PsoC)] a programmable chip according to the present invention.

Figure 4 is a flow chart illustrating steps in a digital operation possible with [the Programmable System On-a-Chip (PsoC)] a programmable chip according to the present invention.

At page 8, lines 2-15:

Reference will now be made in detail to the preferred embodiments of the invention, [PsoC] a programmable mixed analog/digital architecture [(mixed analog/digital)], examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with the preferred embodiments, it will be understood that they are not intended to

limit the invention to these embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims. Furthermore, in the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be obvious to one of ordinary skill in the art that the present invention may be practiced without these specific details. In other instances, well-known methods, procedures, components, and circuits have not been described in detail so as not to unnecessarily obscure aspects of the present invention.

At page 10, lines 3-14:

The present invention provides an on-chip integration of programmable digital and analog circuit blocks in a microcontroller that are able to communicate with each other. Figure 1 is a block diagram 100 illustrating [the Programmable System On-a-Chip (PsoC)] a programmable architecture (exemplified by a programmable "system-on-a-chip" microcontroller such as the PSoC™ microcontroller, available commercially from Cypress MicroSystems, Inc., Bothell, Washington, or from the world wide web at http://www.cypressmicro.com/), composed of programmable analog blocks 121 that can communicate with programmable digital blocks 122 by means of a programmable interconnect structure 123 and a General Purpose I/O 124. This novel architecture allows a single chip solution to perform numerous complex activities that would otherwise require multiple chips or separate applications. The dashed line 120 encloses the four major components 121, 122, 123 and 124 constructed on the single semiconductor chip.

An important aspect of the present invention is the integration of both programmable analog circuits and programmable digital circuits on the same semiconductor chip.

At page 12, lines 2-8:

Figure 2 illustrates one embodiment of the hardware routing resources 200 of the [Programmable System On-a-Chip (PsoC)] programmable chip architecture according to the present invention. Twelve analog amplifier circuits, four ACT circuits 220, four SC1 circuits 221 and four SC2 circuits 222, correspond to the Analog SoCblocs 121 illustrated in Figure 1. Analog signals are coupled to the semiconductor chip at port 0, 212, which consists of four input pins 210 and four output pins 211.

At page 13, line 18 through page 14, line 7:

Figure 3 is a flow chart illustrating steps 300 in a combined analog/digital operation possible with [the Programmable System On-a-Chip (PsoC)] a programmable array according to the present invention. Component reference numbers used are as assigned in Figure 2. An analog signal to be digitized is presented in step 310 at one of the pins of the analog port 0, 210 in Figure 2. Under control of the Analog Clock 205, the analog input signal is coupled in step 320 via a MUX 215 to the input of an SC1 amplifier 221 configured as an integrator with an internal comparator. In step 330, the output of the SC1 amplifier 221 is represented as a digital input signal which is applied to two MFBs 230 configured as an eight bit digital counter. Under the control of the Interrupt Controller 206 and System Clocks 207, the two MFBs 230 accumulate

and store the digital conversion of the analog input signal in step 340. The resulting digital data is then coupled in step 350 via the Independent Internal I/O Bus 240 to a digital output port such as port 0, 241 in Figure 2.

At page 14, line 10 through page 15, line 8:

Figure 4 is a flow chart illustrating steps 400 in a digital operation possible with [the Programmable System On-a-Chip (PsoC)] a programmable array according to the present invention. Component reference numbers used are as assigned in Figure 2. In the present example, a series of pulses taken from an external device are to be counted and a signal is to be coupled to an output device when the count is found to be equal to a preset value. In step 410, the external series of pulses is coupled to a predetermined port and pin, such as pin 1 of port 0, 241 in Figure 2. In step 420, the Independent Internal I/O Bus 240 is used to couple the input signal to an MFB 230. Under control of the Interrupt Controller 206 and the System Clocks 207, the MFB 230 counts pulses in sequence and compares the count to a stored preselected count. When the accumulated count equals the stored count, the MFB generates a signal which is coupled in step 450 to a preselected output port and pin by the Independent Internal I/O Bus 240. It is to be appreciated that a series of pulses taken from an external device that are not satisfactory digital signals could be entered as an analog signal which is then routed through an analog amplifier ACT 220, SC1 221 or SC2 222 in order to produce a digital signal that is then routed to a designated MFB 230.

The preferred embodiment of the present invention, [PSoC] a programmable microcontroller architecture (mixed analog/digital), is thus described. While the present invention has been described in particular embodiments, it should be appreciated that the present invention should not be construed as limited by such embodiments, but rather construed according to the below claims.

IN THE ABSTRACT

Please replace the original abstract with the following Abstract:

A microcontroller with a mixed analog/digital [Programmable System On-a-Chip (PSoC)] architecture including multiple digital [PsoC] programmable blocks and multiple analog [PSoC] programmable blocks in a communication array having a programmable interconnect structure. The single chip design is implemented by integration of programmable digital and analog circuit blocks that are able to communicate with each other. Robust analog and digital blocks that are flash memory programmable can be utilized to realize complex design applications that otherwise would require multiple chips and/or separate applications. The [PSoC] programmable chip architecture includes a novel array having programmable digital blocks that can communicate with programmable analog blocks using a programmable interconnect structure. The programmable analog array contains a complement of Continuous Time (CT) blocks and a complement of Switched Capacitor (SC) blocks that can communicate together. The analog blocks consist of multi-function circuits programmable for one or more different analog functions, and fixed function circuits programmable for a fixed function with

variable parameters. The digital blocks include standard multi-function circuits and enhanced circuits having functions not included in the standard digital circuits. The [PSoC] programmable array is programmed by flash memory and programming allows dynamic reconfiguration. That is, "on-the-fly" reconfiguration of the [PSoC] programmable blocks is allowed. The programmable analog array with both Continuous Time analog blocks and Switched Capacitor analog blocks are offered on a single chip along with programmable digital blocks. The programmable interconnect structure provides for communication of input/output data between all analog and digital blocks.

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